

A Modified SEPIC Converter Fed Induction Motor Drive

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Abstract: Single phase ac-dc PFC bridgeless modified SEPIC rectifier with multiplier stage can be used to improve the efficiency at low input voltage and to reduce the switch-voltage stress. The absence of an input rectifier bridge and the presence of only two semiconductor switches during each switching cycle results in less conduction losses and improved voltage gain compared to the conventional full bridge topology. Operation in DCM enables the converter to achieve higher power factor and lesser total harmonic distortion (THD) of input current. Voltage stress over the whole range of input voltage is less than the conventional boost and SEPIC converters. The two power switches driven by the same control signal significantly simplifies the control circuitry. The bridgeless modified-SEPIC converter with higher overall efficiency and higher power density can be used to drive an induction motor drive, which has a wide range of applications in industrial fields. The performance of this converter can be verified by using SIMULINK/MATLAB.

Keywords: Bridgeless rectifier, discontinuous conduction mode (DCM), power factor correction, modified SEPIC rectifier, total harmonics distortion (THD).

Index Terms: PV panel, auxiliary heating coil, controlled blowers, humidity sensor, solar collector, temperature sensor, microcontroller.

I. Introduction

The demands for improved power factor and reduced total harmonic distortion (THD) in the current drawn from utility are expanding. With the strict requirements of power factor correction (PFC) in power electronic devices, remarkable efforts have been made on the developments of efficient PFC converters. In order to meet harmonic regulations and standards for electronic equipments, power supplies with active power factor correction techniques are becoming necessary. PFC rectifiers have wide range of industrial applications, telecommunication and biomedical fields. Bridgeless converter configurations for PFC have gained importance in the past decade due to their high efficiency [1]. The front-end diode bridge rectifier is eliminated in these configurations which reduce the conduction losses associated in them. Full bridge power supplies with active power factor correction techniques cannot provide a high voltage gain due to the simultaneous conduction of three semiconductor switches at any instant of time. In response to these concerns, significant research efforts have been focused on the development of efficient bridgeless PFC circuit topologies. Compared to conventional PFC circuits, current flows through minimum number of switches in bridgeless PFC circuit. Most power factor correction topologies so far implement a boost-type circuit configuration at its front end [2] because of its low cost, simple circuitry and better performance in terms of efficiency and power factor. However, the boost converter suffers from lower efficiency and higher total harmonic distortion for universal input voltage applications. Compared to other converters, SEPIC rectifier has several advantages such as step up and step down capabilities of output voltage and the magnetic coupling that will lead to reduction in input current ripple [3]. PFC topologies based on Cuk [4] and buck-boost [5] converters have been published. However, these topologies have an inverting output.

SEPIC is essentially a boost converter followed by a buck-boost converter, having the advantages of non-inverted output [6] and being capable of true shutdown when the switch is turned off. The SEPIC converter combines the best qualities of both the boost converter and flyback converter [7]. This converter will reduce current ripples at the input for low level DC outputs, thus eliminating the need for a high frequency filter at the AC side, and the voltage stresses on the switches are reduced. A modified SEPIC converter for high-power-factor rectifier and universal input voltage applications [8] has been proposed to increase the static gain at low input voltage without extreme duty-cycle and with reduced switch voltage stress. This has been achieved by introducing a voltage multiplier cell (D_M and C_M) in the basic SEPIC converter. This topology utilizes input full bridge rectifier resulting in higher conduction losses because the current flows through at least two diodes at any instant of time. A snubber circuit is used in addition to decrease the switching losses. A new single-phase ac-dc PFC bridgeless modified single-ended primary inductor converter (SEPIC) with multiplier stage has been designed to improve the efficiency at low input voltage and reduce the switch-voltage stress. The

absence of input rectifier bridge and the presence of only two semiconductor switches in the path of current flow during each switching cycle results in less conduction losses. A MOSFET with lower R_{DS-on} can be used as the power switch due to lower switch voltage stress. High power factor and low THD of the input current of the converter can be achieved by operation in discontinuous conduction mode (DCM). The DCM operation gives additional advantage of zero-current turn-on in the power switches. The voltage gain can be extended independent of the duty cycle operation. Hence the converter is made suitable for universal line voltage applications. The bridgeless modified SEPIC converter with coupled magnetic configurations results in higher overall efficiency and power density. Inheriting the aforementioned advantages, the converter can be used to drive an induction motor drive which can be used for different applications like conveyers, compressors, mixers etc. The bridgeless modified SEPIC converter is connected to an inverter to drive an induction motor drive. Here the converter acts as an ac-dc converter in the absence of the diode bridge. The three phase voltage source inverter is used as an electronic commutator to operate the drive. The speed of the motor drive is controlled to achieve the voltage control at dc link proportional to the desired speed of the induction motor drive.

1. Operation of the Bridgeless Modified Sepic Pfc Topology

Fig.1 shows the bridgeless PFC modified SEPIC converter with voltage multiplier cell. The bridgeless configuration reduces the conduction losses. The multiplier cell (D_1, C_3 and D_2, C_3) used in the circuit increases the gain and reduces the switch voltage stress. Hence, the bridgeless modified SEPIC topology enhances the overall efficiency. The circuit consists of two symmetrical configurations, each configuration operating in a half cycle. By providing two slow diodes D_p and D_n , the output ground is always connected to the input terminals of ac supply. The three different inductors can be magnetically coupled into a single magnetic core to obtain an input current with very low ripples. Hence, the noise level of generated EMI is greatly minimized, eliminating the requirement of input filter. The converter utilizes two power switches (Q_1 and Q_2). Switch Q_1 is turned ON/OFF during the positive half-line cycle and current flows back to the source through Diode D_p . Switch Q_2 is switched ON/OFF during the negative half-line cycle, with the current flowing back through diode D_n . Both Q_1 and Q_2 can be driven by the same control signal, which significantly simplifies the control circuitry.

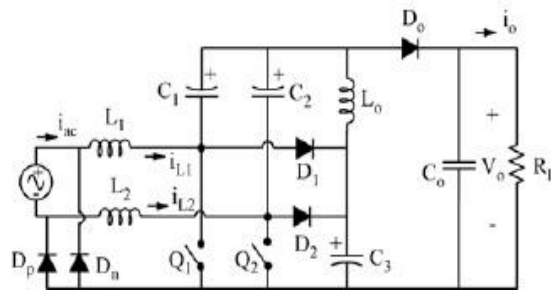


Fig.1. Bridgeless modified SEPIC converter.

II. Operating Modes

Since the bridgeless modified SEPIC converter consists of two symmetrical configurations, the circuit operation is analyzed for the positive half cycle alone. Assuming the three inductors are operating in DCM, the circuit operation during one switching period T_s in a positive half cycle can be divided into three operating modes.

Stage I: Q_1 is ON

In this stage, switch Q_1 is turned-on by the control signal. Both diodes D_1 and D_0 are reverse biased. The three-inductor currents increase linearly at a rate proportional to the input voltage V_{ac} .

Stage II: Q_1 is OFF

During this stage, switch Q_1 is turned-off. Both diodes D_1 and D_0 will conduct simultaneously. The three inductor currents decrease linearly at a rate proportional to the capacitor C_1 voltage V_{C1} . This stage ends when the sum of the currents flowing in the inductors adds up to zero. Then diodes D_1 and D_0 are reverse biased.

Stage III: DCM mode

In this stage, switch Q_1 remains turned-off and both diodes D_1 and D_0 are reverse biased. Diode D_p provides a path for i_{L0} . The three inductors behave as current sources, which keeps the currents constant. Hence, the voltage across the three inductors is zero. This period ends when switch Q_1 is turned-on initiating the next turn-on of the switching cycle. Fig. 2 illustrates the theoretical DCM waveforms during one switching period T_s for the converter.

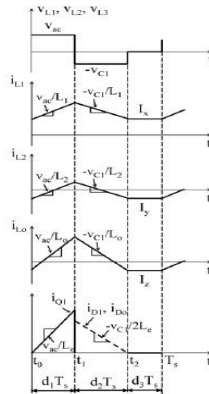


Fig.2.Theoretical waveforms for one switching period of the converter.

Table I: Components Used And Specification

Parameters	Specification
L_1 and L_2	2.2 mH
L_0	180 μ H
C_1, C_2 and C_3	1.2 μ F
C_0	1000 μ F
D_p and D_n	—
D_1, D_2 and D_0	—
Q_1 and Q_2	—

III. Simulation Results

A. Closed loop simulation

(a) Simulation model

The circuit was simulated in MATLAB/SIMULINK. The closed loop simulation of the converter with constant output is shown in Fig.3. Closed loop helps to maintain required output voltage automatically and keep it constant when input changes. The bridgeless modified SEPIC converter works for an input voltage of 120V AC and generate constant output voltage of 415 V. Simulation results of input and output voltages and currents are shown in Fig.4.a.

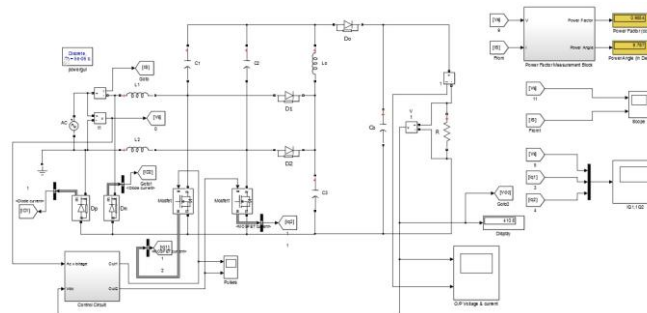


Fig.3. Closed loop simulation diagram of bridgeless modified SEPIC converter

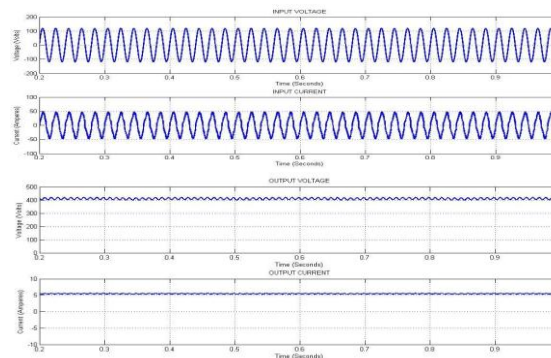


Fig.4.a. Input and output voltages and currents of the closed loop simulation

(b) THD Analysis

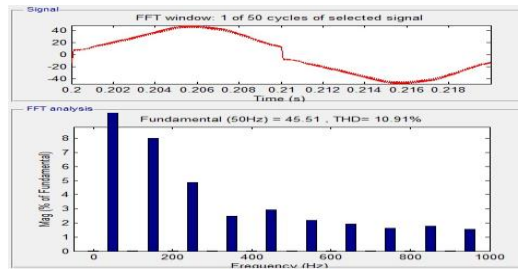


Fig.4.b.i. Simulated and experimental harmonic spectrum for input line current of the converter at an input voltage of 120 Vrms.

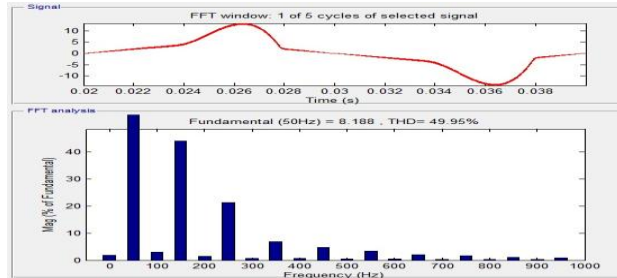


Fig.4.b.ii. Simulated and experimental harmonic spectrum for input line current of the conventional full bridge converter at an input voltage of 120 Vrms.

The THD analysis of the bridgeless modified SEPIC PFC converter shown in Fig.4.b.i indicates that the harmonic content of the input current is 10.91% which is much less than that of the conventional topology, having the THD of input current as 49.95%, as shown in Fig.4.b.ii.

B. Circuit simulation

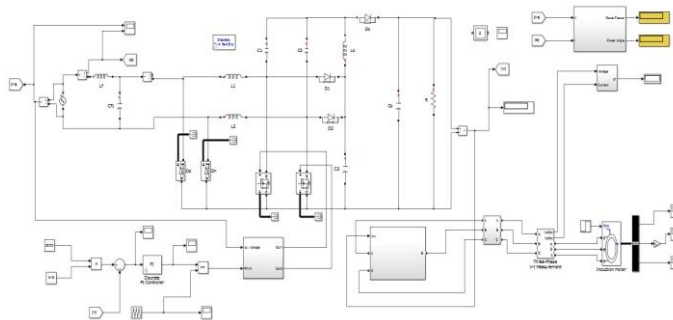


Fig.5. Simulation diagram of bridgeless modified SEPIC PFC converter fed induction motor drive. The converter has been simulated using MATLAB for the following input and output data specifications: $V_{ac} = 120$ V_{rms}, $V_o = 415$ V, $P_{out} = 200$ W, and $f_s = 50$ kHz. Specification of induction motor is as follows: $V_{in} = 415$ V, speed = 1500 rpm, $P_{out} = 5$ HP. Simulation results of input and output voltages and currents of the converter fed induction motor drive are shown in Fig. 6. Speed and torque curves are illustrated in Fig. 7 and Fig. 8 respectively. Fig. 9 illustrates the stator current of the induction motor drive.

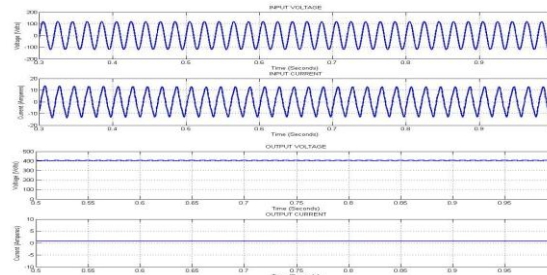


Fig.6. Input and output voltages and currents of the bridgeless modified SEPIC PFC converter fed induction motor drive

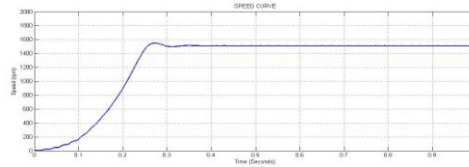


Fig.7. Speed curve of the bridgeless modified SEPIC PFC converter fed induction motor drive

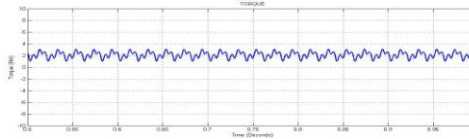


Fig.8. Torque curve of the bridgeless modified SEPIC PFC converter fed induction motor drive

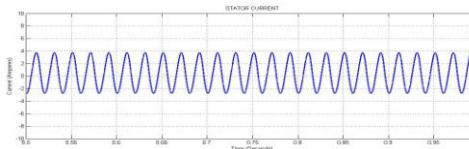


Fig.9. Stator current of the bridgeless modified SEPIC PFC converter fed induction motor drive

IV. Experimental Results

As seen from Fig.6, the input voltage and input current are in phase and almost sinusoidal. Therefore power factor will be almost unity. Output voltage and output current are constant values. $V_{out} = 415$ V, $I_{out} = 1$ A. From Fig.7 and Fig.8, speed and torque of the induction motor drive are found to be constant values at 1500 rpm and 2 Nm respectively. Fig.9 shows that the stator current of the induction motor drive is sinusoidal. Power factor of the bridgeless converter is 0.99, while that of the conventional topology was found to be 0.86. Hence, it has been verified that the bridgeless modified SEPIC PFC converter have improved power factor and less input current THD than that of the conventional full bridge converters.

V. Conclusion

Bridgeless PFC based on modified SEPIC has been presented. Higher power factor and reduced total harmonic distortion of the input current can be achieved. The bridgeless modified SEPIC topology exhibits lower voltage stress over the whole input voltage range, and improved voltage gain and less conduction losses than the conventional SEPIC and boost converters. The two power switches driven by the same control signal significantly simplifies the control circuitry. The conventional scheme has greater losses and ripple. Hence the bridgeless modified SEPIC PFC converter can drive an induction motor drive efficiently. The closed loop operation of and the working of the converter fed induction motor drive has been validated using simulation and verified by experimental results.

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